Design of Carry Skip Adder Using Han Carlson Adder for Low Power and High Speed VLSI Applications

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ABSTRACT

Adders are the basic building block in the arithmetic circuits. In order to achieve high speed and low power consumption a 32bit carry skip adder is proposed. In the conventional technique, a hybrid variable latency extension is used with a method called as parallel prefix network (Brent-Kung). As a result, larger delay along with higher power consumption is obtained, which is the main drawback for any VLSI applications. In order to overcome this, Han Carlson adder along with CSA is used to design parallel prefix network. Therefore it reduces delay and power consumption. The proposed structure is designed by using HSPICE simulation tool. Therefore, a lower delay and low power consumption can be achieved in the benchmark circuits.

Keyword: High speed, low delay, efficient power consumption and size.

I. INTRODUCTION

Adders are a key building block in arithmetic and logic units (ALU) to increasing the speed and reduce the power consumption using Ripple carry adder in existing method area and the delay of the structure is increased by the number of transistor used in carry skip adder (CSKA).In CI-CSKA structure of Mux is replaced by skip logic. It is based on AOI/OAI and it reduced the delay and power consumption. Parallel prefix adder is a technique to increasing the speed of operation, but having some drawbacks. In order to overcome this Hans Carlson adder is used to parallel prefix network, to improve the speed, power consumption and chip area are efficient.

II. RELATED WORKS

[1].S. Sri Katyayani, proposed “Design of Efficient Han-Carlson-Adder” in that,the parallel prefix adder is replaced as speculative HAN-CARLSON ADDER is introduced to reduce the complexity of adder design. [2]. K. Monica, proposed a “Performanceof Delay, Power and Area for Parallel Prefix Adders with Xilinx” in that, KSA, STA, BKA, SKA are done. [3].B. Ram Kumar proposed “Low Power and area efficient carry select adder” in that it evaluates the performance of delay, area, power and their product by hand with logical effort and through custom design and layout in 0.18µm CMOS process technology. [4].Swapna K. Gedam, proposed “parallel prefix Han-carlson adder” In this paper, a modified Parallel Prefix Han-Carlson Adder is introduced which uses different stages of Brent-Kung and Kogge-Stone adders which reduces the complexity of the adder design. [5].

Darjn Esposito proposed “Variable Latency Speculative Han-Carlson Adder” in thatit describes the stages in which variable latency speculative prefix adders can be subdivided and presents a novel error detection network that reduces error probability. [6]. Kai Chirac, proposed “A Static Low-Power, High-Performance 32-bit Carry Skip Adder” in that the adder architecture decreases power consumption by reducing the number of logic levels, glitches, and transistors. To achieve balanced delay, input bits are grouped unevenly in the carry chain. [7].V. Muralidharan proposed “An Enhanced Carry Elimination Adder for Low Power VLSI Applications” in this paper, a great improvement in speed performance and power consumption is achieved. By operating shifting and addition in parallel, the error tolerant adder tree compensates for the truncation errors.[8] Manjunatha G D proposed” Design and implementation of faster parallel prefix kogge stone adder “in this paperKogge-Stone is one of the fastest parallel prefix adders, it eliminated the redundant Black-Cells and performed rerouting thus minimizing the logic delay and routing delay.

III. EXISTING METHOD

In conventional structure of the CSKA due to mux the area and the delay of the structure is increased by the number of transistor used by it. In CI-CSKA structure of Mux is replaced by skip logic. It is based on AOI/OAI and it reduced the delay and power consumption. Due to skip logic the carry generation is complemented then the number of gates used by the AOI/OAI is large compare to conventional method. The RCA has the simplest structure with the smallest area and power consumption but with the worst critical path delay. Adder of a ripple carries sum and carry bits of any half adder stage is not valid, until the carry input of that stage occurs. Propagation delays inside the logic circuitry are the reason behind this. Propagation delay is time elapsed between the application of an input and occurrence of the corresponding output. In the CSLA, the speed, power consumption, and area usages are considerably larger than those of the RCA. 32 bit carry skip adder is used in parallel prefix adder. The Carry skip adder only considers the 8-bit for parallel prefix adder. This parallel prefix adder uses Brent Kung adder. There are different types of the parallel prefix algorithms that lead to different PPA structures with different performances. As an example, Brent Kung adder is one of the fastest structures but there is large power consumption and area usage. Structure of this hybrid variable latency CSKA is given below

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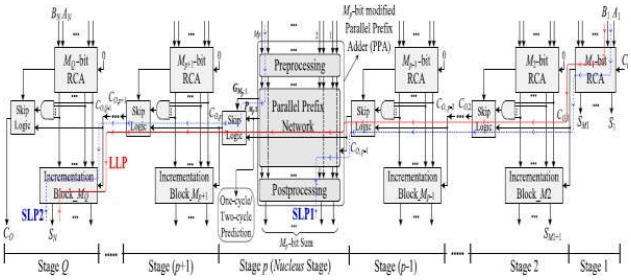


Fig. No. 1

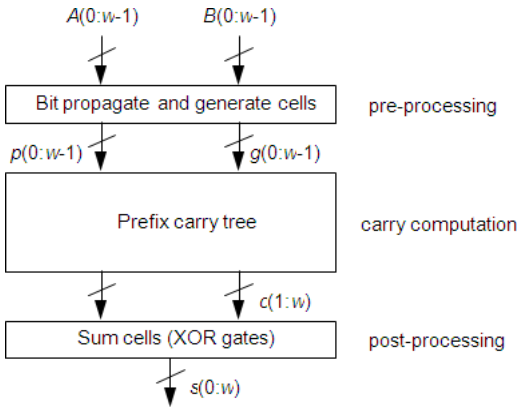
IV. PROPOSED METHOD

The Brent Kung adder is replaced with Han Carlson adder in the place of PPA. It is a combinational of both Brent Kung and Kogge stone adders. The Brent Kung adder provides low area but the speed and power consumption of the adder is high. Similarly in Kogge stone adder speed and area increased. So proposed method combine the both adders in order to reduce the delay and provide efficient power consumption and chip area.

The proposed adder consists of mainly three stages. They are:

- pre-processing stage
- carry computation
- post-processing stage

A. **Block Diagram Of Ppa With Han Carlson Adder:**



Step.1 Pre-processing stage

It takes inputs (a, b) and compute generate and propagate bits which is used for carry generation using below equations,

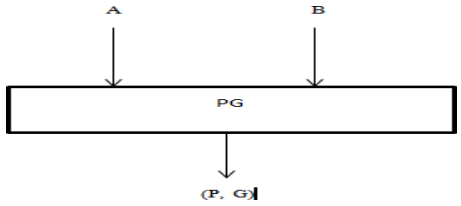


Fig. No. 3

G= a. b
P=a XOR b

Step.2 Carry computation

a. Black cells

Black cell take two pairs of input signals (pi, gi,) and (pj, gj).
It calculates propagate and generate bits for two pair of (pj, gj) signals from right and left block using below equations.

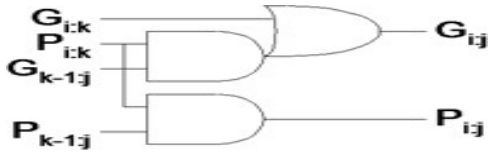


Fig. No. 4

g=gi+pigj
P=pi.pj

Mainly the carry generation network consist of three cells

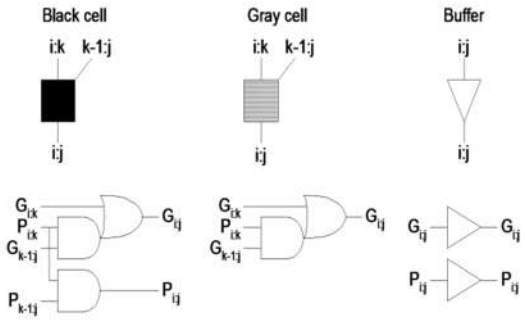
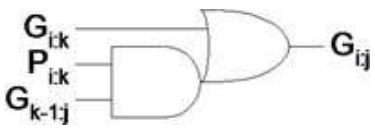


Fig. No 5

b. Gray Cell

This block takes two pairs of input signals (gi, pi) and (gj, pj) and generates the single output signal g. The gray cell will execute only the generate bit.



c. Buffer cell

Buffer is uses the pair of input signals (gi, pi) and passes the same signals to the output g=gi, & p= pi.

Step. 3 Post Processing Stage

In the post processing stage we are computing the sum using the previously generated carry and the propagate bits. In this proposed system, the adders pre-compute the carry which is used for eradicate the carry propagation problems. And also decrease the delay of the adders. The lateral stage used in the proposed adder is Kogge-stone adder in which the redundant black cells are reduced in each stage which will reduce the power consumption. Thus there will be betterment in the power and delay while using the proposed adder.

V. STRUCTURAL DIAGRAM OF HAN CARLSON ADDER

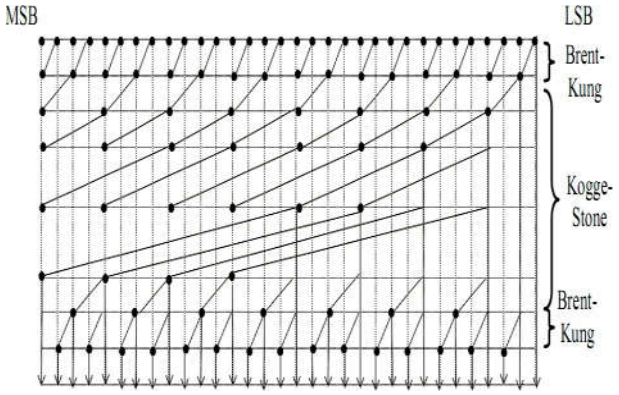


Fig. No. 7

Parallel prefix based BKA provides a better tradeoff between delay and area. But power consumption is more. KSA Provide delay reduction and area improvements. But the cost of high power consumption is the main disadvantage of the KSA. Han Carlson adder it is one of the parallel prefix adder, used to improve the speed and efficient area power consumption. To design Parallel Prefix Hybrid Han-Carlson Adder (HCA) it differs from other adder in that it can be used for large word Sizes. The proposed system design reduces the number of prefix operation by using more number of Brent-Kung (BK) stages and lesser number of Kogge-Stone(KS)stages. This also reduces the Complexity, silicon area and power consumption significantly. Here we are using only Black cells. Then, Two inputs are given to the XOR&AND gate (a&b). If both inputs are high AND the carry. If anyone input is high XOR operation propagates the carry.

VI. EXPRIMENTAL RESULT

Simulation was performed using the modelsim and Xilinx version 12.3tool. Area and delay were directly obtained from software and area was measured in terms of number of transistors used in design.

Table1.Comparison of Adders

	Brent kung adder	Han Carlson adder
Power	0.137W	0.120W
Area(Number of 4 input LUTs)	95	93
Delay	16.422ns	16.115ns

A. Simulation Results using modelsim software the output analysis for various structures of carry skip adder was obtained and it is shown in figure.

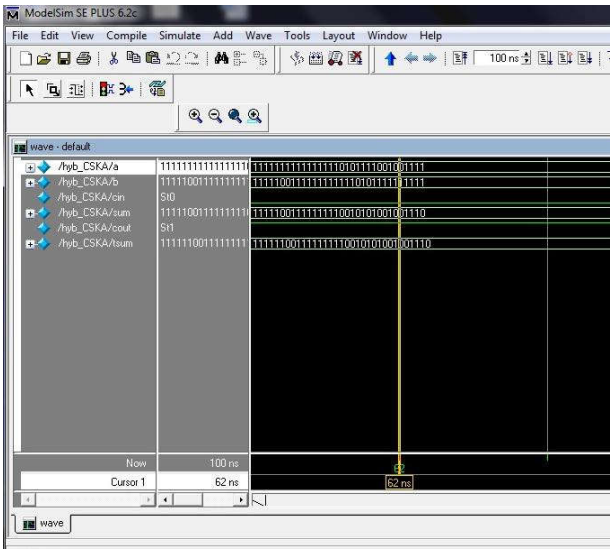


Fig. No.8

CONCLUSION

In proposed system Han Carlson adder is used to improve the speed.8-bit parallel prefix adder is used in the Brent kung adder, having some delay and power consumption to overcome this, here the Brent kung adder replaced by 8-bit Han Carlson adder, so that the power and delay will be improved. Compare with the existing system power and delay is reduced.

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